EXHIBIT C

D:\NU_fp_lib_original_modules_june_2002\floatlib_old\add_sub.vhd

```
--============================================================--
--                                                            --
--  NORTHEASTERN UNIVERSITY                                   --
--  DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING         --
--  RAPID PROTOTYPING LABORATORY                              --
--                                                            --
--  FILE          | add_sub.vhd                               --
--  --------------+-----------------------------------        --
--  DESCRIPTION   | Module to perform addition or             --
--                | subtraction.                              --
--  --------------+-----------------------------------        --
--  AUTHOR        | Pavle Belanovic                           --
--  --------------+-----------------------------------        --
--  DATE          | 20 June 2002                              --
--                                                            --
--============================================================--

--************************************************************************--
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--                                                                        --
--************************************************************************--

--============================================================--
--                         LIBRARIES                          --
--============================================================--

-- IEEE Libraries --
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

-- float
library work;
use work.float_pkg.all;

------------------------------------------------------------
--                   Add/Sub Module                       --
------------------------------------------------------------
entity add_sub is
    generic
    (
        man_bits            :   integer :=
    );
    port
    (
```

D:\NU_fp_lib_original_modules_june_2002\floatlib_old\parameterized_priority_encoder.vhd

```
1   --============================================================--
2   --                                                            --
3   --  NORTHEASTERN UNIVERSITY                                   --
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5   --  RAPID PROTOTYPING LABORATORY                              --
6   --                                                            --
7   --  FILE          | parameterzied_priority_encoder.vhd        --
8   --  --------------+-----------------------------------        --
9   --  DESCRIPTION   | Parameterized priority encoder            --
10  --  --------------+-----------------------------------        --
11  --  AUTHOR        | Pavle Belanovic                           --
12  --  --------------+-----------------------------------        --
13  --  DATE          | 20 June 2002                              --
14  --                                                            --
15  --============================================================--
16
17  --****************************************************************************--
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34  --                                                                            --
35  --****************************************************************************--
36
37  --============================================================--
38  --                        LIBRARIES                           --
39  --============================================================--
40
41  -- IEEE Libraries --
42  library IEEE;
43  use IEEE.std_logic_1164.all;
44  use IEEE.std_logic_arith.all;
45  use IEEE.std_logic_unsigned.all;
46
47  -- float
48  library work;
49  use work.float_pkg.all;
50
51  ------------------------------------------------------------
52  --          Parameterized priority encoder                --
53  ------------------------------------------------------------
54  entity parameterized_priority_encoder is
55      generic
56      (
57          man_bits        :   integer :=  0;
58          shift_bits  :   integer :=  0
59      );
60      port
61      (
```

```
105     --connect output signals
106     OUT1(exp_bits+man_bits_out)                                          <=
        s_out;
107     OUT1(exp_bits+man_bits_out-1 downto man_bits_out)   <=  e_out;
108     OUT1(man_bits_out-1 downto 0)                                        <=
        f_out;
109
110     --instatiate components
111     --normalizer
112     norm: normalizer
113         generic map
114         (
115             exp_bits            =>  exp_bits,
116             man_bits            =>  man_bits_in
117         )
118         port map
119         (
120             --inputs
121             MAN_IN              =>  f_in,
122             EXP_IN              =>  e_in,
123             READY                   =>  READY,
124             CLK                     =>  CLK,
125             EXCEPTION_IN    =>  EXCEPTION_IN,
126             --outputs
127             MAN_OUT             =>  f_int,
128             EXP_OUT             =>  e_int,
129             EXCEPTION_OUT   =>  exc_int,
130             DONE                    =>  rd_int
131         );
132     --round_add
133     rnd_add: round_add
134         generic map
135         (
136             man_bits_in     =>  man_bits_in,
137             man_bits_out    =>  man_bits_out
138         )
139         port map
140         (
141             --inputs
142             MAN_IN              =>  f_int,
143             READY                   =>  rd_int,
144             CLK                     =>  CLK,
145             ENABLE              =>  round_int,
146             EXCEPTION_IN    =>  exc_int,
147             --outputs
148             MAN_OUT             =>  f_out,
149             EXCEPTION_OUT   =>  EXCEPTION_OUT,
150             DONE                    =>  DONE
151         );
152     --SYNCHRONOUS
153     main: process (CLK)
154     begin
155         if(rising_edge(CLK)) then
156             --pipelining sign bit
157             s_out           <=  s_int;
158             s_int           <=  s_in;
159             --pipelining exponent
160             e_out           <=  e_int;
161             --pipelining rounding
162             round_int   <=  ROUND;
163         end if;--CLK
```

```
164         end process;--main
165     end rnd_norm_arch;--end of architecture
166
```